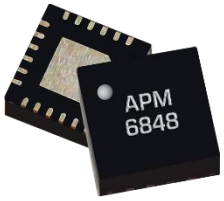
2-30 GHz Surface Mount Low Phase Noise Amplifier APM-6848SM



1. Device Overview

1.1 General Description

The APM-6848SM is an integrated 2-stage broadband, low phase noise LO driver amplifier designed to provide a saturated +20 dBm output power from a 0-6 dBm input power with low DC power consumption, packaged in a 4mm QFN. This amplifier uses GaAs HBT technology for low phase noise, and is optimized to provide enough power to drive the LO port of an S-diode mixer from 2 GHz to 20 GHz or an H or L diode mixer from 2 GHz to 32 GHz. This amplifier can be operated with a variety of bias conditions including VC=VB=5V for both low power and high power applications.

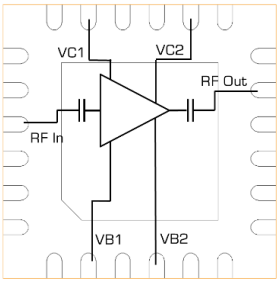
1.2 Features

- -165 dBc/Hz phase noise at 10 kHz offset frequency
- Power and gain control
- +22 dB gain
- Low DC power consumption
- Positive-only biasing
- No sequencing required
- Unconditionally stable
- Integrated DC blocks – No bias-tees or off-chip blocking required

1.3 Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G Transceivers
- Driver amplifier for S, H, and L – diode mixers
- Suitable as a T3 mixer driver

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
APM-6848SM	4x4 mm Surface Mount	QFN	**RoHS**	Active	EAR99
EVAL-APM-6848SM	Connectorized Evaluation Fixture	EVAL	**RoHS**	TBD, Contact Support	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

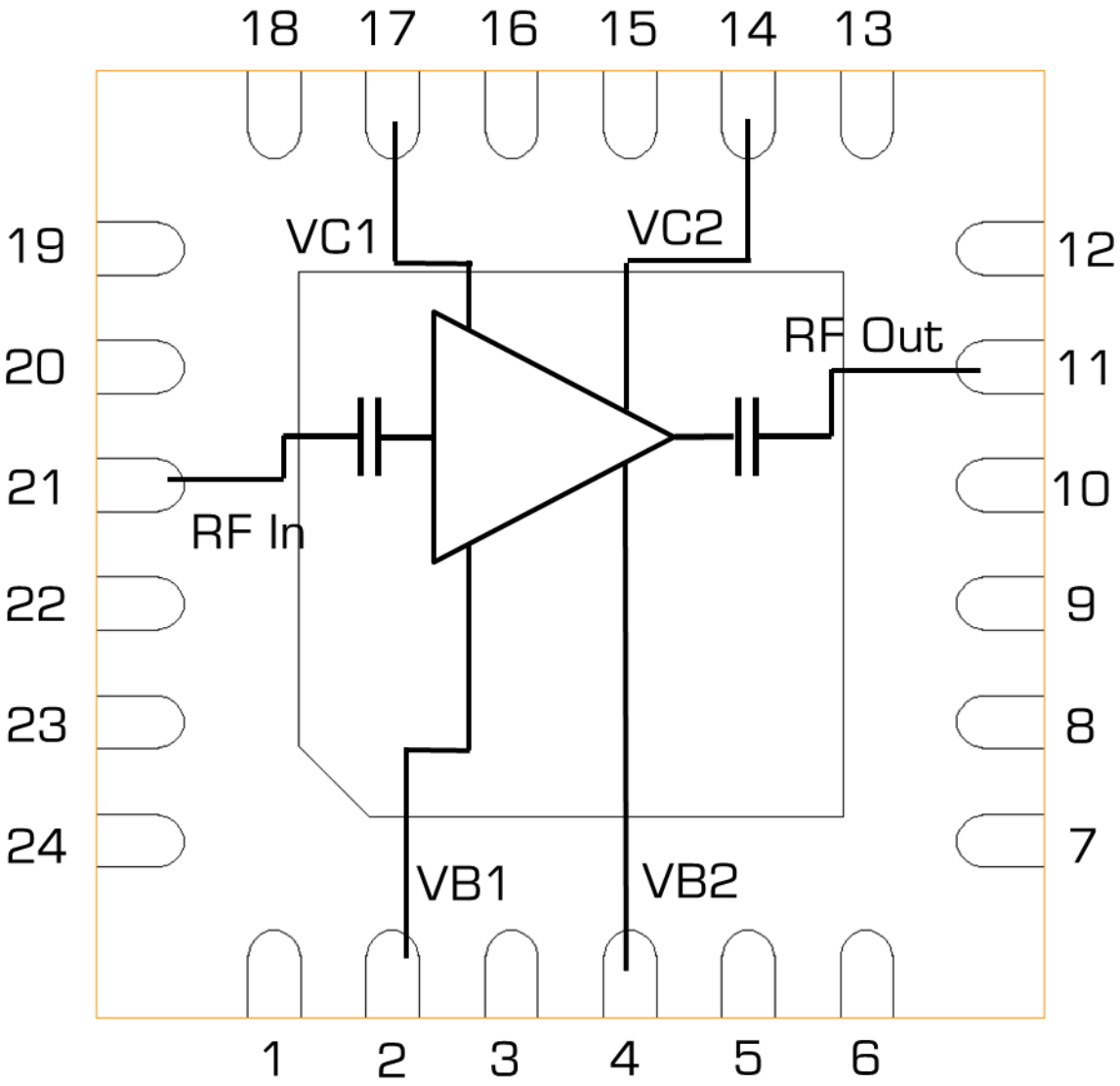
Revision History

Revision Code	Revision Date	Comment
-	December 2019	Datasheet Initial Release

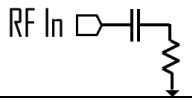
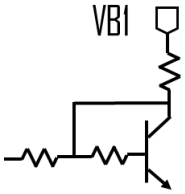
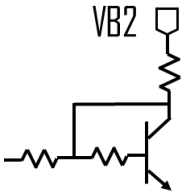
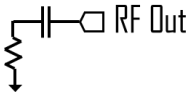
2. APM-6848 Port Configurations and Functions

2.1 APM-6848SM Port Diagram

A top-down port diagram of the APM-6848SM is shown below.



2.2 APM-6848SM Port Functions

Pin	Function	Description	Equivalent Circuit for Package
21	RF Input	This is the RF Input port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω.	
17	Collector Supply Port 1	Pad VC1 is the DC voltage supply pad for the 1st stage of the amplifier IC. See section 3.6 for performance at different bias conditions.	
14	Collector Supply Port 2	Pad VC2 is the DC voltage supply pad to the 2nd stage of the amplifier IC. Larger VC voltage will result in larger power consumption and larger power output. See section 3.6 for performance at different bias conditions.	
2	Base Supply Port 1	Pad VB1 is the DC voltage supply pad for a current mirror which controls the collector current of the 1st stage (Ic1). Larger voltages result in a higher current draw through pad VC1, effectively functioning as a gain control pin for the 1st stage of the amplifier. See section 3.6 for performance at different bias conditions.	
4	Base Supply Port 2	Pad VB2 is the DC voltage supply pad for a current mirror which controls the collector current of the 2nd stage (Ic2). Larger voltages result in a higher current draw through pad VC2, effectively functioning as a gain control pin for the 2nd stage of the amplifier. See section 3.6 for performance at different bias conditions.	
11	RF Output	This is the RF Output port of the amplifier die. It is internally DC blocked and RF matched to 50 Ω. Must have less than 7:1 VSWR when operating with voltage larger than 5V on VC1 or VC2.	
GND	Ground	Backside of the IC must be connected to a DC/RF ground with high thermal and electrical conductivity.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Collector Positive Bias Voltage (VC, VC1, VC2)	7	V
Positive Bias Current (Ic, Ic1+Ic2)	300	mA
Current Mirror Positive Bias Voltage (VB, VB1, VB2)	7	V
Current Mirror Positive Bias Current (Ib, Ib1+Ib2)	8	mA
RF Input Power	+20	dBm
Output Load VSWR	7:1	-
Operating Temperature	-40 to +125	°C
Storage Temperature	-65 to +150	°C
θ_{JA}	TBD	°C/W

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD
Weight	EVAL-APM-6848SM	43.7g

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

	Min	Nominal	Max[2]	Units
T_A, Ambient Temperature	-40	+25	+125	°C
Positive DC Voltage (VC1)	+3	+5	+6	V
Positive DC Current (Ic1)	8	21	40	mA
Positive DC Voltage (VC2)	+3	+5	+6	V
Positive DC Current (Ic2)	8	21	40	mA
Positive DC Current Mirror Voltage (VB1)	+3	+5	+6	V
Positive DC Current Mirror Current (Ib1)	0.9	2	2.6	mA
Positive DC Current Mirror Voltage (VB2)	+3	+5	+6	V
Positive DC Current Mirror Voltage (Ib2)	0.9	2	2.6	mA

3.4 Sequencing Requirements

There is no sequencing required to power up or power down the amplifier.

Amplifier must have an output load connected when operating with a VC1, or VC2 voltage larger than +5V.

[2] Maximum recommended operating current conditions without RF input applied. Please see typical performance plots on page 12 for relationship between RF input power and DC current draw.

3.5 Electrical Specifications[3]

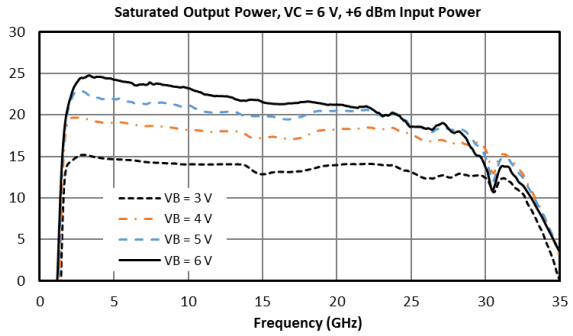
The electrical specifications apply at T_A=+25°C in a 50Ω system.

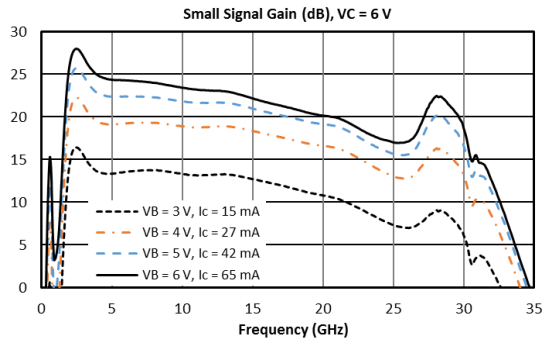
Parameter	Test Conditions	Frequency	Min	Typical	Max	Units
Frequency			2		30	GHz
P_{sat}	5V/5V bias, +6 dBm Input Power	2 GHz – 20 GHz	18	+21		dBm
		20 GHz – 29 GHz	14	+18		
Small Signal Gain	5V/5V bias, -25 dBm Input Power	2 GHz – 20 GHz	18	22		dB
		20 GHz – 29 GHz	15	18		
Input Return Loss		2 GHz – 20 GHz		14		
		20 GHz – 29 GHz		7		
Output Return Loss		2 GHz – 20 GHz		16		
		20 GHz – 29 GHz		11		
Noise Figure		2 GHz – 26.5 GHz		6		
Reverse Isolation		2 GHz-29 GHz		62		
Collector Current[4], Ic	5V/4V	-		27		mA
	5V/5V	-		43		
	5V/6V	-		67		
Current Mirror Current, Ib	5V/4V	-		2.9		
	5V/5V	-		4		
	5V/6V	-		5.2		
Input IP3 (IIP3)	5V/5V bias, -25 dBm Input Power	2 GHz – 29 GHz		-2		dBm
Output IP3 (OIP3)		2 GHz – 29 GHz		+20		
Output P_{1dB}	5V/5V bias	2 GHz – 20 GHz		+19		
		20 GHz – 29 GHz		+15		
Input Power for Saturation	5V/5V bias	2 GHz – 29 GHz		+4		dBm
Phase Noise @ 10 kHz Offset	5V/5V bias, +9 dBm Input power, 4 GHz	2-20 GHz		-165		dBc/Hz

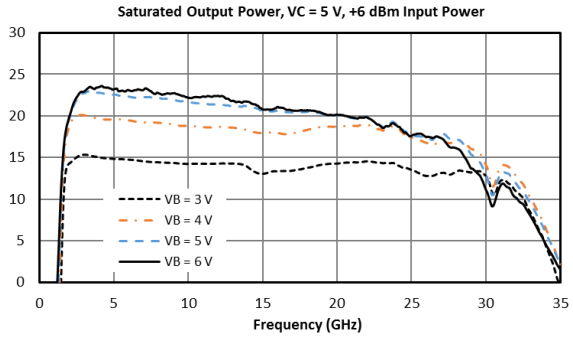
[3] All Specifications and performance shown with VC1 = VC2 and VB1 = VB2

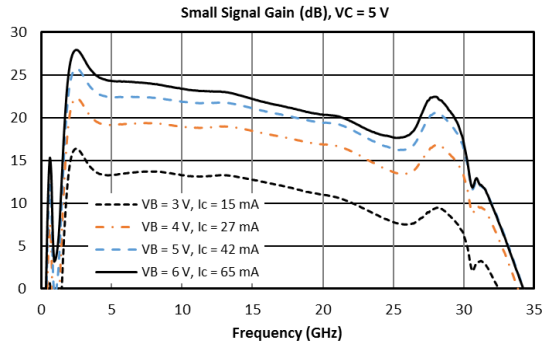
[4] Bias conditions for Ic and Ib tested with no RF input power. See section 3.6 for DC current vs. RF power. Bias conditions presented as VC/VB.

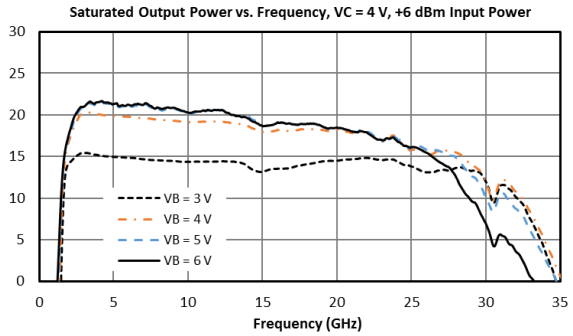
3.6 APM-6848SM Typical Performance Plots[5]

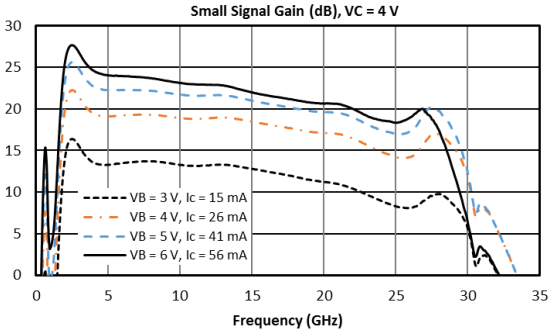


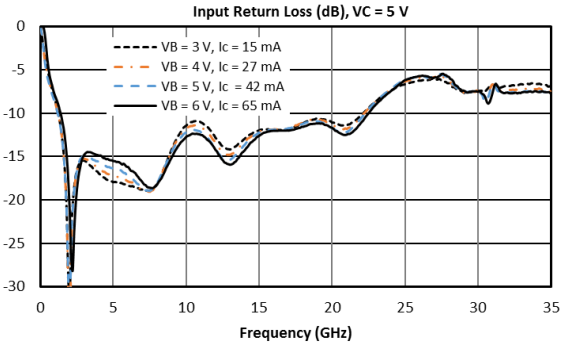


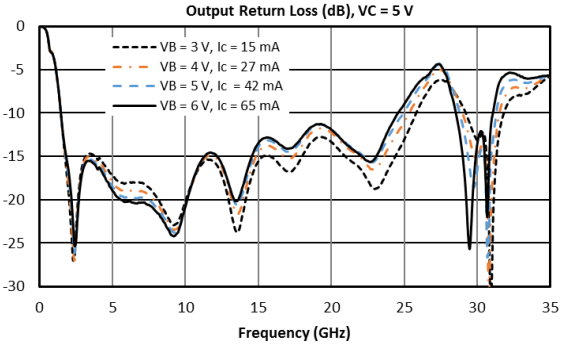




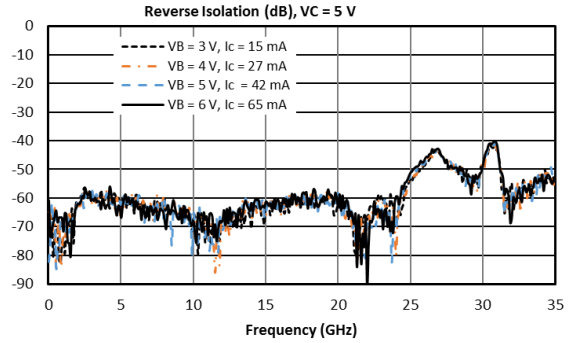


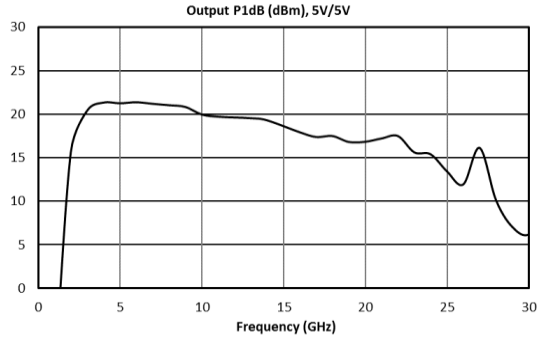


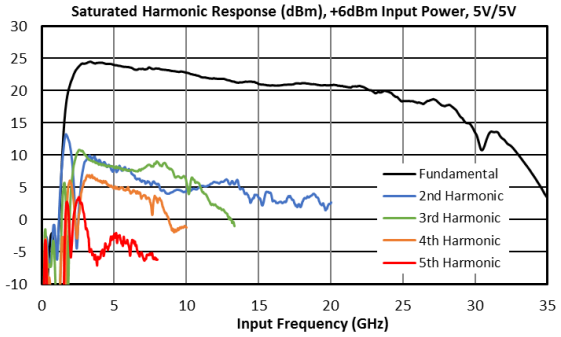


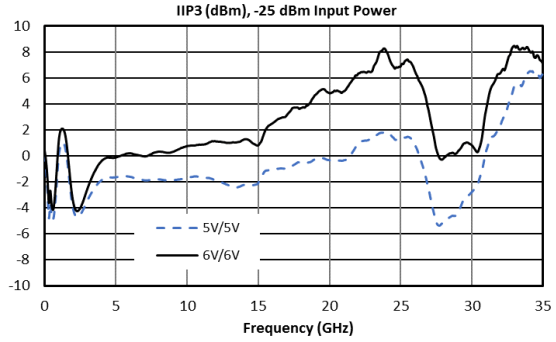


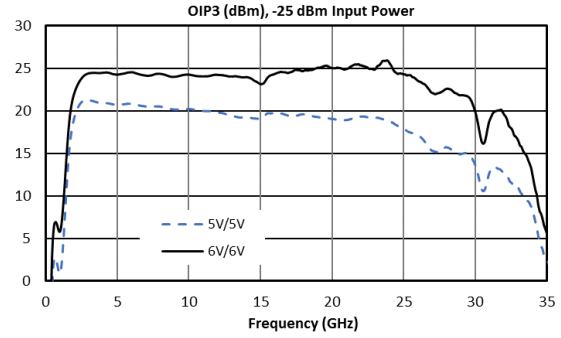
[5] Surface mount performance plots are taken in the EVAL-APM-6848 connectorized fixture, and include launch, line, and connector insertion losses.

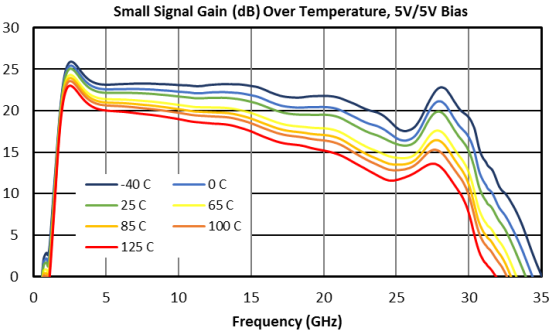


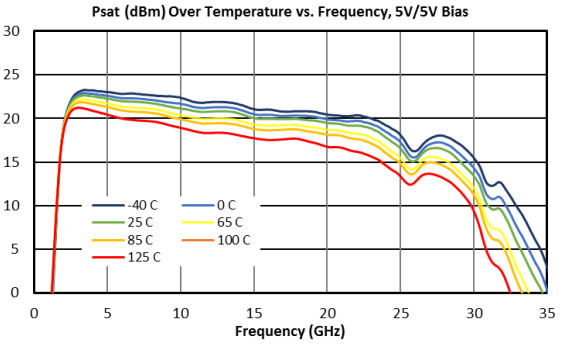


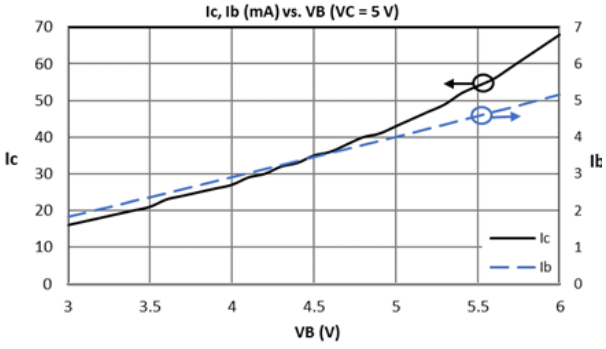




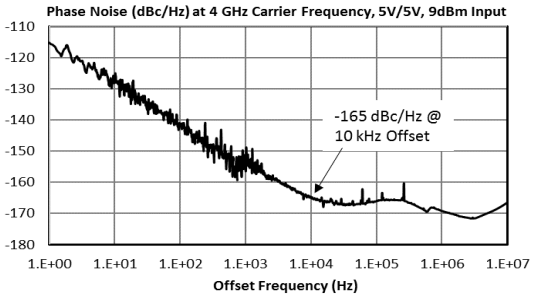


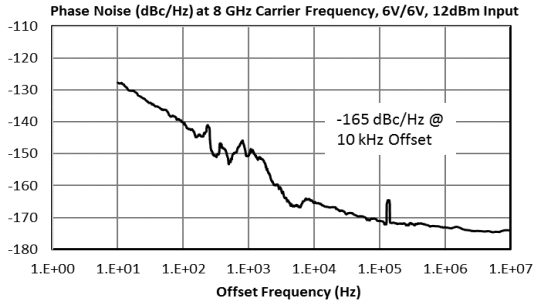


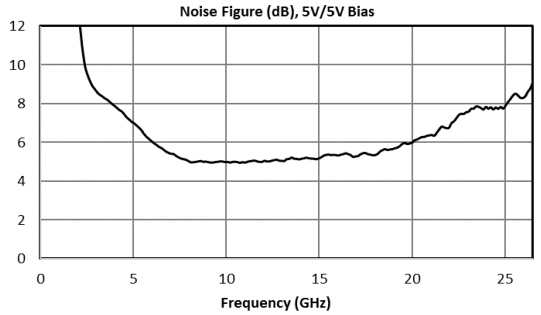


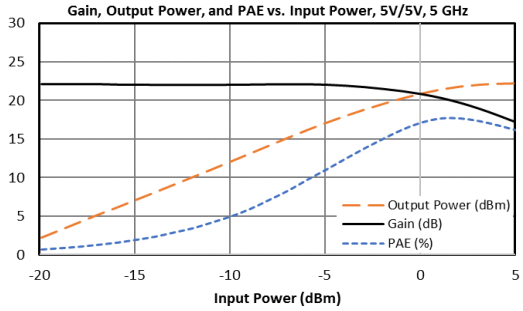


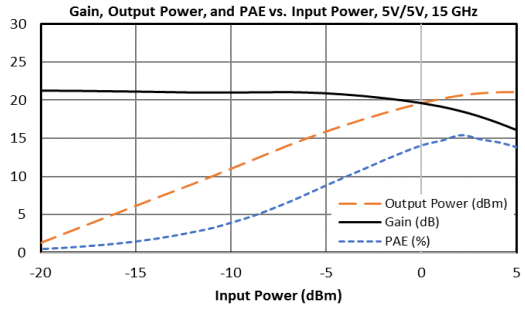
3.7 Connectorized Module APM-6848PA Performance Plots[6]

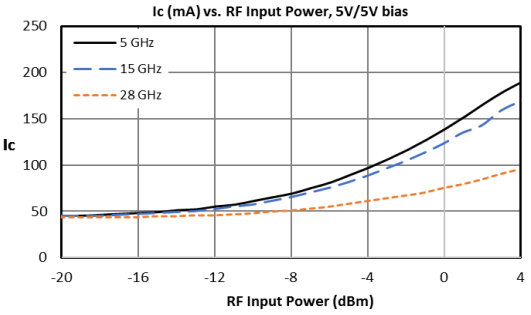






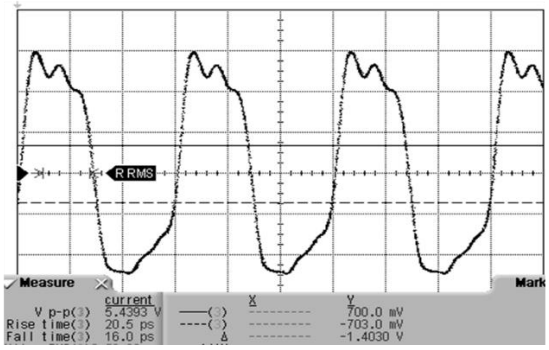




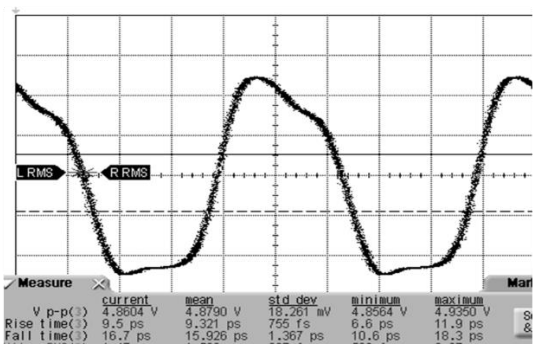


3.8 Time Domain Plots[7]

5 GHz, +5 dBm In, 5V/5V bias



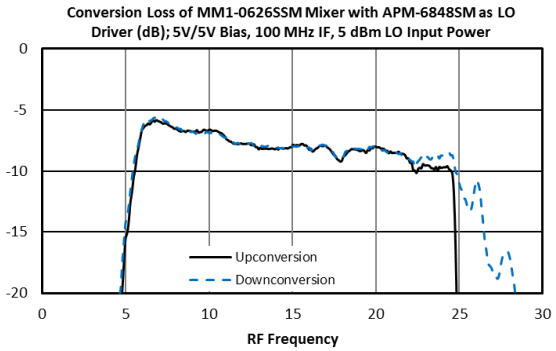
10 GHz, +5 dBm In, 5V/5V bias

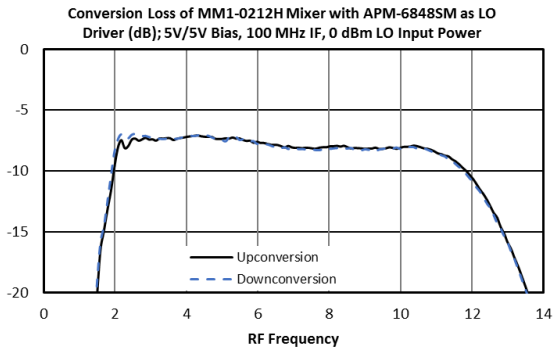


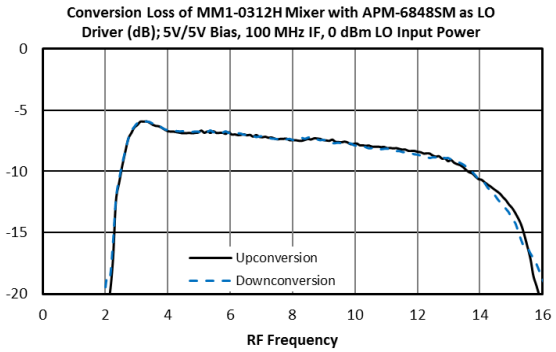
[6] Surface mount module APM-6848SM performance can be expected to be similar to connectorized module performance.

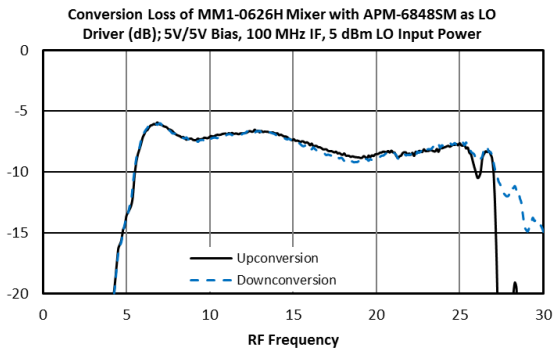
[7] Fast rise time is desirable for linear T3 mixer operation.

3.9 Conversion Loss of Marki Mixers Using APM-6848SM as LO Driver





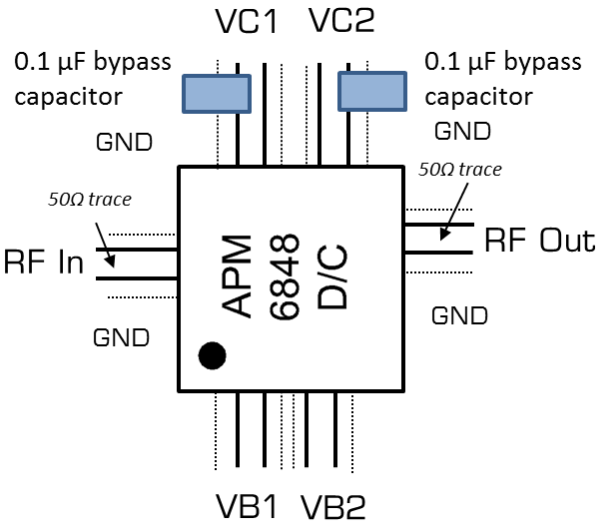




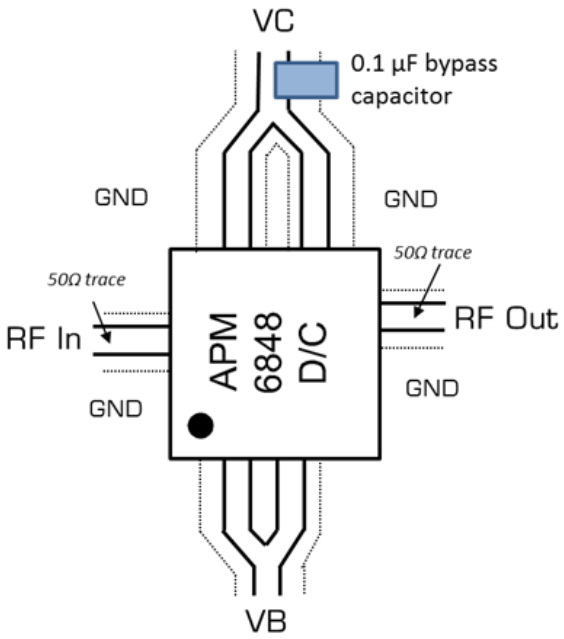
4. Application Information

4.1 APM-6848SM Application Circuit

Below are the recommended application circuits for the APM-6848SM.



RF input and output should be soldered to 50 Ω traces. Since this is a 2-stage amplifier, VC and VB lines may be biased separately at different voltages for improved efficiency (application circuit shown above), or they may be combined for convenience (below). If combined, feedback oscillations can form along the VC supply lines unless sufficient bypass capacitance to ground is used.



4.2 Gain and Power Control

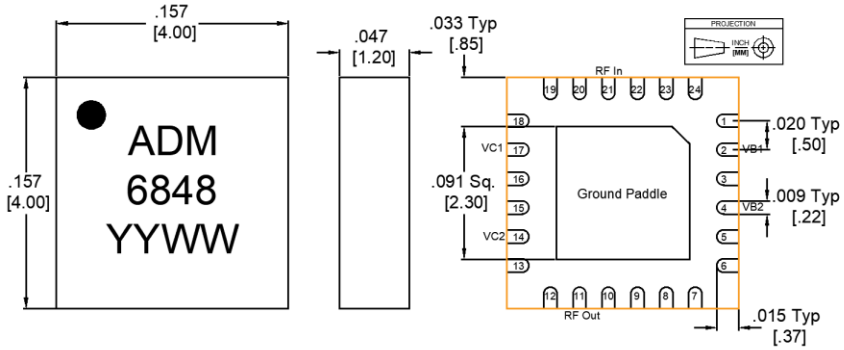
The APM-6848 is a 2-stage amplifier integrated on a single IC. In the APM-6848SM package, the user has some freedom to operate the 2 amplifier stages independently for their application-specific needs. Please refer to section 2.2 to see the function of each port on the APM-6848SM, and refer to the gain and Psat plots in section 3.6 to see how bandwidth, saturated output power, and gain profile change for various bias conditions.

Generally, the gain of the first stage and second stage of the amplifier can be controlled by adjusting VB1 and VB2 respectively. Increasing the voltage applied to a VB pad increases the current drawn into the corresponding amplifier stage, which strongly correlates to the gain of that stage, and some difference to the output power of that stage. Increasing the voltage on a VC pad generally increases the linearity, maximum output power, and DC power consumption of the corresponding amplifier stage.

In the case where a user wants to drive the LO port of a mixer from an initial LO power of +9 dBm at 10 GHz, the user could apply 5V at all 4 DC ports and see an output power of +21.5 dBm and an overall power consumption of about 1 watt (the amplifier stages pull more DC current as the gain compresses in a high input power condition). Alternatively, the user could apply 3.5 V – 4 V to VB1 and VC1, and 6V to VB2 and VC2 and see an output power of 22.5 dBm with very little difference in the overall power consumption. For applications with a strict power budget and performance requirements, optimizing the bias conditions of the amplifier can be a useful tool for the system designer.

5. Mechanical Data

5.1 APM-6848SM Package Outline Drawing



Pad #	Function
1	N/C
2	VB1
3	N/C
4	VB2
5	N/C
6	N/C
7	N/C
8	N/C
9	N/C
10	N/C
11	RF Out
12	N/C
13	N/C
14	VC2
15	N/C
16	N/C
17	VC1
18	N/C
19	N/C
20	N/C
21	RF In
22	N/C
23	N/C
24	N/C

Notes:

1. Substrate material is Plastic.
2. I/O Leads and Die Paddle are 0.05 µm Au over 0.02 µm Pd over 0.5 µm Ni.
3. All unconnected pins should be connected to PCB RF ground.

5.2 APM-6848SM Landing Pattern